10623709
updated

Routing Architecture for a Programmable Logic Device

Cross-Reference to Related Applications

[0001] This is a continuation application of serial number 10/140,287 filed May 6, 2002, is now a U.S. Patent 6,630,842, entitled "Routing Architecture for a Programmable Logic Device" which claims the benefit of U.S. Provisional Application Serial Number 60/289,176, filed May 6, 2001.

Background of the Invention

1. Field of the Invention

[0002] This invention relates generally to integrated circuits and, in particular, to improved routing architectures for a programmable logic device.

2. Description of the Related Art

[0003] A programmable logic device ("PLD") is a digital, user-configurable integrated circuit used to implement a custom logic function. For the purposes of this description, the term PLD encompasses any digital logic circuit configured by the end-user, and includes a programmable logic array ("PLA"), a field programmable gate array ("FPGA"), and an erasable and complex PLD. The basic building block of a PLD is a logic element that is capable of performing logic functions on a number of input variables. A logic element is typically equipped with circuitry to programmably implement the "sum of products" logic or look-up table logic, as well as one or more registers to implement sequential logic. Conventional PLDs combine together large numbers of such logic elements through an array of programmable